REMARKS

Claims 2-6 and 24-38 are pending in the present application. Claims 35-38 have been presented herewith.

Drawings

The drawings have been objected to for the reasons set forth in the Notice of Draftsperson's Patent Drawing Review Form PTO-948, received along with the current Office Action dated April 17, 2003. Correct formal drawings for Figs. 1A, 2A, 3A, 4A and 6A having proper margins has been submitted herewith. The Examiner is respectfully requested to acknowledge receipt and acceptance of the corrected formal drawings.

Claim Rejections-35 U.S.C. 103

Claims 2-6 and 24-34 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, in view of the Doan et al. reference (U.S. Patent No. 5,946,595), the Besser et al. reference (U.S. Patent No. 6,165,903) and the Xiang et al. reference (U.S. Patent No. 6,015,752). This rejection is respectfully traversed for the following reasons.

A feature of the preferred embodiments of the present application is that a silicide layer is formed in a first rapid thermal anneal (RTA) process, the silicide layer is masked with a silicon layer, and then a second RTA process is carried out whereby the

silicon layer provides the amount of silicon contained in the silicide layer of the processed structure. The embodiments of the present application as claimed are used in connection with an SOI substrate, in which a silicon layer is formed on a BOX insulation layer. That is, claim 24 includes in combination "providing a semiconductor substrate which has a silicon region located on an insulating layer formed in the semiconductor substrate". Claim 30 includes in combination "providing a field oxide layer and a silicon on insulator layer on the buried oxide layer".

In view of the use of the supplemental silicon layer, generation of voids in the substrate can be reduced. The embodiments of the present application as claimed are therefore especially useful in connection with an SOI substrate having a thin silicon layer, within the range of 50-100 nm, or less than 70 nm.

Applicant respectfully notes that of the prior art as relied upon in the above noted rejection, only Applicant's admitted prior art as described with respect to Figs. 1A-1C is directed to an SOI structure. However, a supplemental silicon layer is not used in connection with Applicant's admitted prior art. Accordingly, a device including a thin SOI layer with irregular thickness manufactured as in Applicant's admitted prior art, will include thinner parts of the SOI layer that may be salicided entirely to create voids.

Applicant respectfully emphasizes that the various secondary references as relied upon by the Examiner do not teach SOI structures. Particularly, the Besser et al. reference includes a device formed on silicon substrate 30. That is, the secondary references are not concerned with preventing consumption of an SOI layer having

limited silicon available for an RTA process, because the structures of the secondary references are formed on substrates. Applicant therefore respectfully submits that the respective methods for fabricating a semiconductor device of claims 24 and 30 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 2-6 and 24-38 is improper for at least these reasons.

Claims 35-38

Claims 35 and 36 as dependent upon claim 24 further feature the thickness of the silicon region located on the insulating layer formed in the semiconductor substrate. Likewise, claims 37 and 38 as dependent upon claim 30 further feature the thickness of the silicon on insulator layer. Since the secondary references as relied upon by the Examiner are not related to SOI structures, the prior art as relied upon by the Examiner does not make obvious the features of these claims including providing a supplemental silicon layer for use with a silicon region or a silicon on insulator layer of the specified thicknesses. That is, the prior art does not recognize a workable process for use with thin SOI layers.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for

at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.

Andrew J. Telesz, Jr.
Registration No. 33,581

AJT:dmc

VOLENTINE FRANCOS, P.L.L.C.
12200 Sunrise Valley Drive, Suite 150
Reston, Virginia 20191
Telephone No.: (703) 715-0870
Facsimile No.: (703) 715-0877

Enclosures: Five (5) sheets of corrected formal drawings